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Electrical characterization of Au/n-GaN metal–semiconductor and Au/SiO_2/n-GaN metal–insulator–semiconductor structures

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ABSTRACT

In the present work, we have investigated the current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics of Au/SiO_2/n-GaN metal–insulator–semiconductor (MIS) Schottky diode and compared with Au/n-GaN metal–semiconductor (MS) Schottky diode. Calculations showed that the Schottky barrier height and ideality factor of the MS Schottky diode is 0.79 eV (*I–V*), 0.87 eV (*C–V*) and 1.45, respectively. It is observed that the Schottky barrier height increases to 0.86 eV (*I–V*), 0.99 eV (*C–V*) and ideality factor deceases to 1.3 for MIS diode. For the MS diode, the calculated doping concentration is 4.17×10^{17} cm^{-3}. However, in the case of the MIS Schottky diode, the decrease in doping concentration is observed and the respective value is 2.08×10^{17} cm^{-3}. The obtained carrier concentration of the MIS diode is reduced about 50% when compared to the MS diode. The interface state density as determined by Terman's method is found to be 3.79×10^{12} and 3.41×10^{10} cm^{-2} eV^{-1} for the MS and MIS Schottky diodes, respectively. The calculated interface densities are 2.47×10^{11} cm^{-2} eV^{-1}, 3.35×10^{11} cm^{-2} eV^{-1} and 3.5×10^{11} cm^{-2} eV^{-1} for the sweep rates of 300, 450 and 600 mV/s from MOS *C–V* measurements for the MIS Schottky diode. The interface state density calculated from Terman's method is found to be increased with sweep rate. From the *C–V* measurement, it is noted that the decrease in the carrier concentration in MIS diodes as compared to MS diode may be due to the presence of oxide interfacial layer. DLTS measurements have also been performed on MIS Schottky diode and discussed.

1. Introduction

Groups III–V semiconductors, particularly nitrides, including InN, GaN, AlN and their alloys, emerge rapidly as important materials both in research and industrial areas within the last decade. This is due to their many good properties like the efficient, long-lasting light-emitting capability, especially in the visible range, the chemical stability, the mechanical strength and the high temperature endurance [1–6]. Recently, a number of GaN field-effect transistors (FETs) such as hetero-bipolar transistors, metal–oxide–semiconductor hetero-structure FETs and metal–insulator–semiconductor (MIS) FETs have been reported. In particular, the GaN MIS structure equipped with an inversion mode as a minority-carrier channel is important for high-power switching devices since it would provide lower leakage currents and reduce power consumption, enabling normally off operation with high blocking voltage even at high temperatures. For advancement of these devices, the detailed electrical characterizations of metal/GaN Schottky (MS) and metal/insulator/GaN (MIS) interfaces have to be investigated.

Many researchers have explored various metal/insulator schemes for the fabrication of Schottky contacts on GaN [7–13]. Tu et al. [7] fabricated GaN metal–oxide–semiconductor structure using the high-dielectric-constant Ta_2O_5 and possible low threshold voltages were demonstrated with high-frequency *C–V* measurements. Chang et al. [8] prepared silicon nitride (SiN)/GaN MIS diodes by electron cyclotron resonance chemical vapor deposition (ECR-CVD). They showed that the interface densities were less than 4×10^{11} cm^{-2} eV^{-1} around the mid-gap and the minimum value was 5×10^{10} cm^{-2} eV^{-1} at 0.6 eV below conduction band edge. Nakano and Jimbo [9] investigated the electrical characterization of SiO_2/GaN metal–insulator–semiconductor diodes by using *C–V* technique and reported a total interface trap density of $\sim 2.2 \times 10^{12}$ cm^{-2} eV^{-1}. Bae et al. [10] fabricated Al-gate n-GaN/nitride-thin-Ga_2O_3/SiO_2 and n-GaN/Si_3N_4 MIS capacitors that were evaluated by capacitance–voltage (*C–V*) measurements. They showed that n-GaN/Si_3N_4 structures posses a significantly higher density of electron trap levels than n-GaN/nitride-thin-Ga_2O_3/SiO_2 structures. Tsai et al. [11] studied the hydrogen sensing and response characteristics of Pt/GaN and Pt/SiO_2/GaN Schottky diode under different concentration of hydrogen gases in a wide

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temperature range in an air atmosphere. They reported that the Pt/SiO_2/GaN (MIS) Schottky diode had higher hydrogen detection capability and larger Schottky barrier height modulation in an air atmosphere in comparison with the Pt/GaN (MS) Schottky diode. Hu et al. [12] evaluated the capacitance–voltage characteristics of GaN metal–insulator–semiconductor (MIS) diodes at 150 °C. They reported that a high density of SiO_2/GaN interface traps was found to pin the semiconductor surface potential (Φ_s) at 0.7–0.9 eV from *C*–*V* scan at 150 °C.

Some of the researchers were also reported DLTS measurements on GaN MIS devices. For instance, Cho et al. [13] investigated the deep level spectra in a series of undoped GaN films with different GaN buffer growth rates. They observed two distinct deep levels with activation energies of $E_1 = 0.19 - 0.23$ eV and $E_2 = 0.50 - 0.60$ eV below the conduction band. Matocha et al. [14] fabricated metal–oxide–semiconductor gallium nitride capacitors on c-plane and m-plane GaN, reported that the capacitance–voltage hysteresis was less on m-plane compared to c-plane GaN surfaces. They also suggested a lower interface-state density at the m-plane GaN/SiO_2 interface.

In this work, an attempt is made to investigate the detailed electrical transport properties of GaN Schottky diodes with and without an interfacial oxide layer using forward bias *I*–*V* characteristics and reverse bias *C*–*V* measurements. Finally, the interface state density is evaluated for the GaN MIS and MS structures. Further, the trap carrier concentration and activation energy of trap in the GaN MIS Schottky diodes are determined by DLTS technique.

2. Experimental details

2 μm thick Si-doped GaN layer is grown on a c-plane Al_2O_3 sapphire substrate by metalorganic chemical vapor deposition (MOCVD). The carrier concentration is determined to be 4.07×10^{17} cm^{-3} by means of Hall measurements. Before metallization, the two pieces of n-GaN films are ultrasonically degreased with warm trichloroethylene followed by acetone and methanol for 5 min each. It is then dipped into boiling aquaregia [HNO_3:HCl = 1:3] for 10 min to remove the surface oxides and then rinsed in deionized (DI) water. For ohmic contacts, we used the standard e-beam deposited Ti/Al (25 nm/100 nm) and annealed at 650 °C in N_2 ambient for 3 min. First the Au (50 nm) Schottky contact with a diameter of 0.7 mm is deposited through stainless steel mask using e-beam evaporation on one of the piece of GaN film. A 20 nm thick SiO_2 layer is deposited on the other piece of GaN film followed by 50 nm thick Au by electron beam evaporation system. Au evaporation processes are carried out in a vacuum coating unit at a pressure of about $5–6 \times 10^{-6}$ mbar. The current–voltage (*I*–*V*) and capacitance–voltage characteristics of Au/n-GaN (MS) and Au/SiO_2/n-GaN (MIS) Schottky contacts are measured using Keithley source measuring unit 2400 and automated DLTS (DLS-83D) system at room temperature. Also, MOS *C*–*V* measurements of MS and MIS are carried out by automated DLTS system. Finally, DLTS measurements are performed in the temperature range 100–400 K by placing the samples (MIS) inside liquid nitrogen cryostat to evaluate trap parameters by automated DLTS-83 D system (Semilab, Lock-in amplifier based system which facilitated measurement at pulse frequency in the mHz range).

3. Results and discussion

3.1. Current–voltage characteristics

The current–voltage characteristics are used widely to study the performance of the Schottky contacts since they offer many important device parameters. Fig. 1 shows the forward and reverse biased curves of Au/n-GaN (MS) and Au/SiO_2/n-GaN (MIS) Schottky diodes at room temperature. For forward bias and $V > 3kT/q$, the following equation describe the *I*–*V* characteristic of the Schottky diode according to the thermionic emission theory [15]

$$I = I_o \exp\left(\frac{q(V - R_S I)}{nkT}\right) \quad (1)$$

where saturation current I_o is expressed by

$$I_o = AA^{**}T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \quad (2)$$

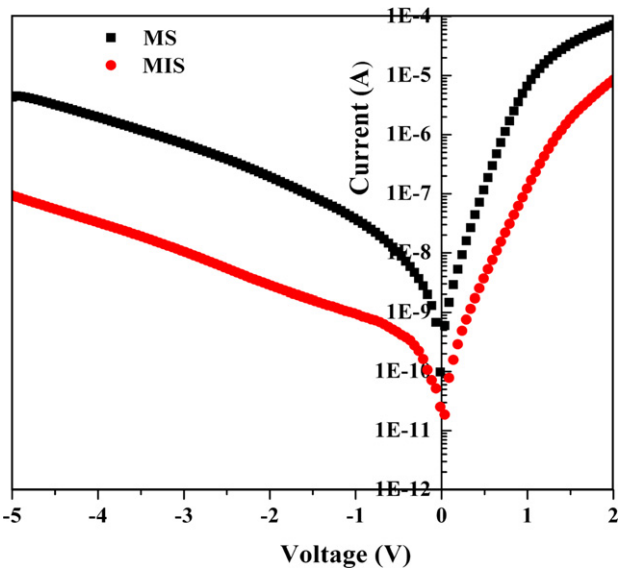

Fig. 1. Typical current–voltage characteristics of the Au/n-GaN MS and Au/SiO_2/n-GaN MIS diodes at room temperature.

where *q* is the electronic charge, *T* the measurement temperature in Kelvin, *n* the ideality factor, A^{**} the effective Richardson constant (by using an effective mass of 0.22 m_e for n-GaN [16,17], the value of A^{**} is calculated to be 26.4 A cm^{-2} K^{-2}), *k* the Boltzmann's constant, R_S the series resistance, Φ_b the zero-bias barrier height and *A* the contact area.

Using a linear curve fit to the forward characteristics in Fig. 1, the barrier height (Φ_b) and ideality factor (*n*) can be calculated. The ideality factor is a measure of the conformity of the diode to be pure thermionic emission and is determined from the slope of the forward bias ln (*I*) versus *V* characteristics through the relation,

$$n = \frac{q}{kT}\frac{d(V - IR_S)}{d(\ln I)} \quad (3)$$

The ideality factors of MS and MIS Schottky diodes are found to be 1.45 and 1.30, respectively. The ideality factor is determined from the plot of natural log of current versus forward bias voltage for small forward currents where the effect of series resistance is small (current ranges: of 9.281×10^{-9} to 3.586×10^{-6} A for MS Schottky diodes and 4.89×10^{-10} to 8.719×10^{-8} A for MIS Schottky diodes). The value of ideality factors obtained from the forward bias *I*–*V* plot is found to be greater than unity. Such behaviour has been mainly attributed to the particular distribution of the interface states [18], the image force effect, recombination-generation and tunneling may be other possible mechanisms that could lead to an ideality factor value greater than unity [19–24]. Further, it has been reported in the literature [19,20] that an effective layer of nonzero thickness must exist between the metal and semiconductor even when both are in intimate contact. Films of thickness of 10–25 Å usually lead to values of the ideality factor in the range of 1.18–1.30. The ideality factor higher than unity may also be attributed to the oxide layer grown on the semiconductor, suggesting that the potential barriers at real metal–semiconductor interfaces depend much more on the applied voltage than predicted ideal contacts.

The apparent or measured barrier height $q\Phi_b$ is given by

$$q\Phi_b = \frac{kT}{q}\ln\left(\frac{AA^{**}T^2}{I_o}\right) \quad (4)$$

where I_o is measured from the plot of $\ln[I/1 - \exp(-qV/kT)]$ versus *V* (from reverse *I*–*V* characteristics) as an intercept at *V* = 0 (as shown in Fig. 2). The extrapolation of the *I*–*V* plots to zero bias yields the value of saturation current as 5.09×10^{-10} A and 3.12×10^{-11} A for

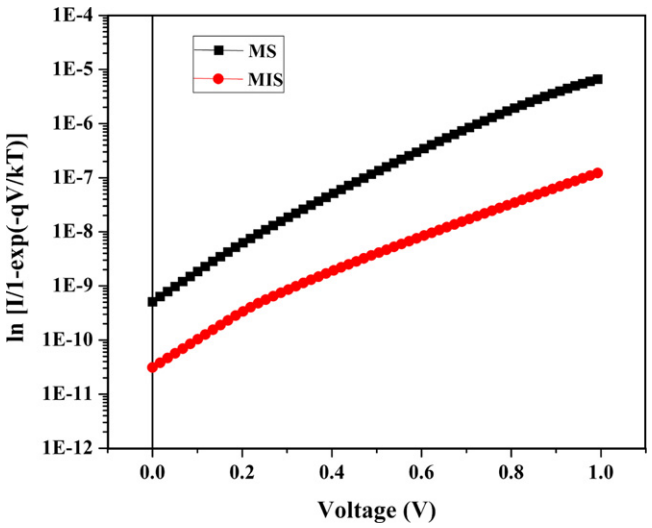

Fig. 2. Plot of $I/[I - \exp(-qV/kT)]$ versus V for the Au/n-GaN MS and Au/SiO_2/n-GaN MIS diodes.

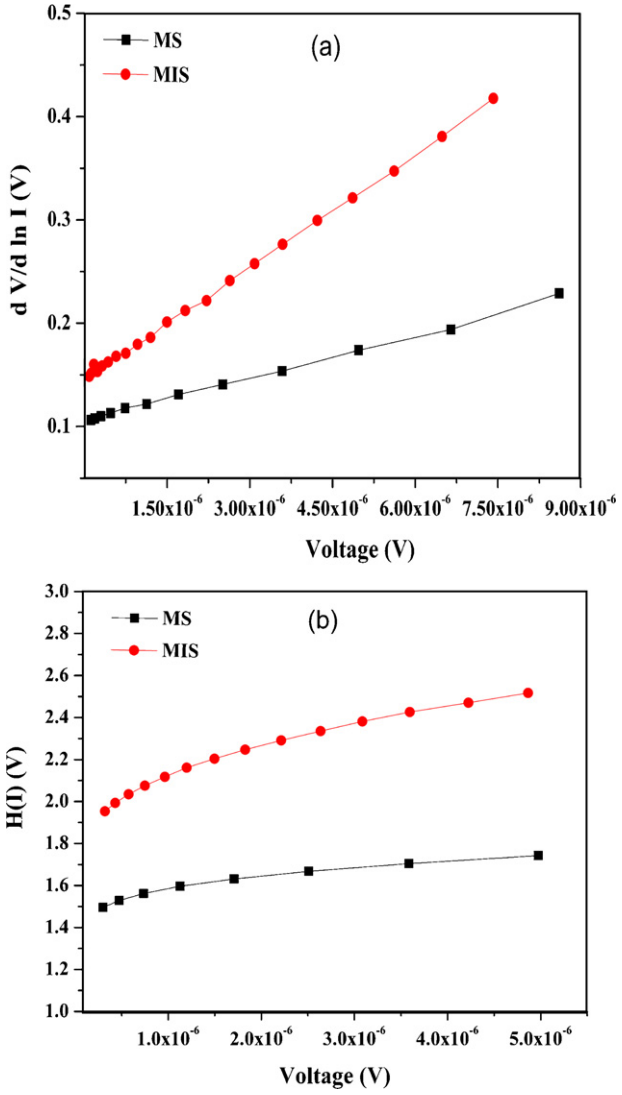

Fig. 3. (a) dV/dln$I$ versus I of Au/n-GaN MS and Au/SiO_2/n-GaN MIS diodes, and (b) $H(I)$ versus I plots of Au/n-GaN and Au/SiO_2/n-GaN MIS diodes.

the MS and MIS Schottky diodes, respectively. Then the presence of intentionally grown insulating layer has reduced the value saturation current I_o by two orders of magnitudes. By using I_o the value Φ_b can be calculated. The value of the barrier height for MS and MIS Schottky diodes are found to be 0.79 eV and 0.86 eV, respectively. The increase in barrier height of the Au/n-GaN Schottky diode with insulating layer could be explained by an increase in negative charges at the interface. These negative charges probably arise due to electron traps localized at the GaN interface and associated with Ga vacancies created near the surface during the formation of insulating layer. Consequently it is clear that the different barrier heights could be due to modified-interface chemistry.

It is clearly observed that there are two regimes of forward current transport in as-deposited Au/n-GaN Schottky contact. The low voltage regime is governed by thermionic emission. The high voltage regime is assumed to be due to some mechanisms other than thermionic emission. The recombination current becomes dominant under low forward bias voltage conditions [25]; however, I–V plot deviate considerably from the linearity due to the effect of series resistance and interface state density at larger forward bias voltages [26]. In addition, the current rises slowly with the applied reverse bias and does not show any effect of saturation. This soft or slight saturating behaviour of reverse current may be explained in terms of the image force lowering of Schottky barrier height and the presence of interfacial insulating layer at metal–semiconductor interfaces [19,21]. Usually, the forward bias current–voltage characteristics are linear in semi-logarithmic scale at low voltage but deviate considerably from linearity due to the effect of parameters such as the bulk series resistance (R_S) and density of interface states (N_{SS}) when the applied bias is sufficiently large. Lower the interface state density and the series resistance, the greater the range over which I–V curve does in fact yield a straight line [27]. As the linear part of the forward I–V plots is reduced, the accuracy of the determination of Φ_b and n becomes lower.

The values of series resistance R_S are calculated by using the method developed by Cheung and Cheung [28] at higher current range (over which the I–V characteristics is not linear). Cheung's functions are given as

$$\frac{dV}{d(\ln I)} = IR_S + n\left(\frac{kT}{q}\right) \tag{5}$$

$$H(I) = V - \frac{nkT}{q}\ln\left(\frac{I}{AA^{**}T^2}\right) \tag{6}$$

and

$$H(I) = IR_S + n\Phi_b \tag{7}$$

should give a straight line for the data of downward curvature region in the forward bias I–V characteristics. The term IR_S is the current drop across the series resistance of Schottky diodes.

Fig. 3(a) shows the experimental dV/dln$I$ versus I plot for the MS and MIS Schottky diodes, respectively. Thus the values of R_S and nkT/q have been obtained from the slope and y-axis intercepts of the dV/dln$I$ versus I plot, respectively. The calculated values of ideality factor are 1.51 and 1.42 for MS and MIS diodes from Fig. 3(a). From Fig. 3(b), it is evident that the plot of $H(I)$ versus I gives a straight line with the y-axis intercept equal to $n\Phi_b$ and the slope parameter can be used to check the consistency of Cheung's method. However, it can be clearly seen (from Table 1) that there is relatively a difference between the values of ideality factor obtained from the downward curvature regions of forward bias I–V plots and from the linear regions of the same characteristics. The reason for this difference can be attributed to the existence of effects such as series resistance and the bias dependence of Schottky barrier height according to the voltage drop across the interfacial layer and change of the interface states with the bias in the low voltage region of the I–V plot.

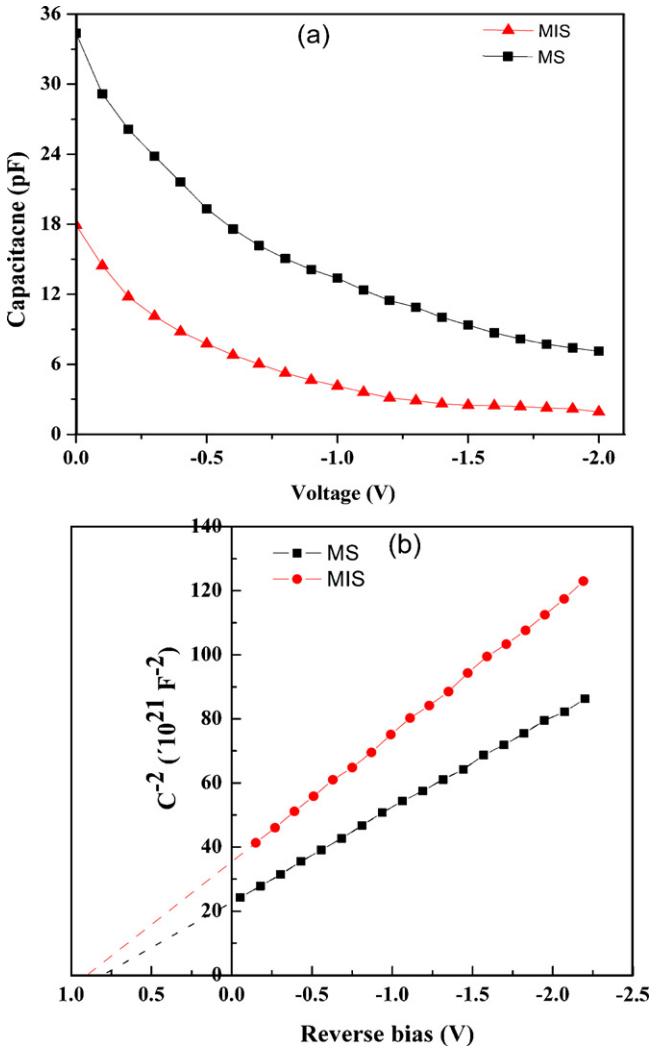

Fig. 4. (a) Capacitance–voltage characteristics of Au/n-GaN MS and Au/SiO_2/n-GaN MIS diodes at 1 MHz frequency, and (b) C^{-2} versus V for the Au/n-GaN MS and Au/SiO_2/n-GaN MIS diodes.

3.2. Capacitance–voltage characteristics

The capacitance–voltage characteristics of MS and MIS n-GaN Schottky diodes are measured in the dark at a frequency of 1 MHz with an ac modulation of 100 mV. Interface states are unable to respond to the ac signal since the reverse bias C–V measurements are made at very high frequency (1 MHz). Fig. 4(a) shows typical C–V curves of Au/n-GaN and Au/SiO_2/n-GaN Schottky diodes. The zero bias capacitance of MS and MIS Schottky diode is seen to drop from 35 pF to 18 pF. The decrease in zero bias capacitance in the case of MIS Schottky contact may be due to the presence of interfacial layer. In order to estimate the barrier height and doping concentration, $1/C^2$ versus V_R plots (Fig. 4(b)) are obtained from the C–V data of Fig. 4(a). In Schottky diodes, with an interfacial layer, the depletion layer capacitance can be expressed as [19]

$$\frac{1}{C^2} = \frac{2(V_R + V_0)}{q\varepsilon_S N_D a^2} \tag{8}$$

where V_R is the reverse bias voltage, V_0 the built-in potential, q the electronic charge and N_D the doping concentration. The diffusion potential or built-in potential is usually measured by extrapolating C^{-2} versus V plot to the x-axis. An insulating film possibly changes these characteristics with bias. The zero bias barrier height from C–V measurement is defined by

$$\Phi_b = V_0 + \frac{kT}{q} + \Phi_n \tag{9}$$

where Φ_n is the Fermi energy measured from the conduction band edge.

For the MS Schottky barrier, the calculated doping concentration and the zero bias barrier height are 4.17×10^{17} cm^{-3} and 0.87 eV, respectively. The doping concentration and zero bias barrier height of the MIS structure are found to be 2.08×10^{17} cm^{-3} and 0.99 eV, respectively. However, in the case of MIS Schottky diode, the increase in zero bias barrier height with decrease in doping concentration is observed. A 50% reduction of the carrier concentration of the MIS diode is obtained compared to the MS diode.

For, the ideal Schottky barrier which is expected from the deviation of C–V data on uniformly doped semiconductor can be attributed to a number of factors including traps in depletion layer, effective contact area variation, interfacial layer and charge in surface states [20,29]. A possible theory [20] that accounts for the apparent decrease in the doping concentration for the MIS diode invokes interface states in equilibrium with the semiconductor. Another possible explanation could be due to traps associated with the oxide. The series resistance values determined from the Cheung's equations, ideality factor and barrier height are given in Table 1.

3.3. Determination of interface states density (N_{SS})

The density of interface states for electrons or holes are always affected by the interfaces and must not necessarily introduce energy levels in the band gap. At high forward bias voltages, the nonlinearity of the I–V characteristics of the MIS Schottky diode indicate the presence of continuum of interface states in equilibrium with the semiconductor [20]. The voltage dependence of effective barrier height Φ_e is contained in the ideality factor, n through the relation

$$\frac{d\Phi_e}{dV} = \beta = 1 - \frac{1}{n(V)} \tag{10}$$

where β is the voltage coefficient of Φ_e. The effective barrier height Φ_e is given by [27]

$$\Phi_e = \Phi_b + \beta V \tag{11}$$

For a MIS diode having interface states in equilibrium with the semiconductor, the ideality factor 'n' becomes greater than unity as proposed by Card and Rhoderick [20] and is given by

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_S}{W_D} + qN_{SS}\right] \tag{12a}$$

Table 1
Various parameters determined from I–V characteristics of MS and MIS n-GaN Schottky diodes.

Sample	Saturation current I_S (A)	Ideality factor 'n' (from I–V)	Ideality factor 'n' (from $dV/d\ln I$ versus I)	Barrier height (eV)	Series resistance (R_S) (Ω)	
					$dV/d\ln I$ versus I	$H(I)$ versus I
MS	5.094E−10	1.45	1.51	0.79	123.99	130.25
MIS	3.115E−11	1.30	1.42	0.86	682.79	788.17

where W_D is the space charge region width being deduced from the experimental C–V measurements at high frequency (1 MHz), N_{SS} is the density of interface states, ε_s and ε_i are the permittivities of the semiconductor and the insulator layer (SiO_2), respectively. The depletion layer (space charge region) thickness is calculated using $W_D = \sqrt{2\varepsilon_s V_{bi}/qN_D}$. The depletion layer width increases until strong inversion layer is formed under reverse bias. For any given semiconductor at a given temperature the depletion layer width depends on doping concentration N_D. The voltage dependent ideality factor $n(V)$ can be expressed as $n(V) = (V/(kT/q))\ln(I/I_S)$ [30]. The expression for the interface state density can be given as

$$N_{SS}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_S}{W_D}\right] \quad (12b)$$

In an n-type semiconductor, the energy of the interface states E_{SS} with respect to the bottom of the conduction band at the surface of the semiconductor is given by [20,31,32]

$$E_C - E_{SS} = q(\Phi_e - V) \quad (13)$$

Eqs. (10)–(13), along with the I–V characteristics can be used for the determination of the interface states density as a function of interface states energy E_{SS} with respect to the bottom of the conduction band.

Substituting the values of voltage dependence of ideality factor n(V) in Eq. (12a), using $\varepsilon_s = 9.5\varepsilon_o$, $\varepsilon_i = 3.8\varepsilon_o$, $\delta = 200$ Å and $W = 6.93$ μm (from C–V measurements) for the MIS diode and $\delta = 10$ Å [33], $W = 1.55$ μm (from C–V measurements) for MS diode, the values of N_{SS} as a function of V are obtained and reported in Table 2. The resulting dependence of N_{SS} is converted to a function of E_{SS} using Eq. (13). N_{SS} versus $E_C - E_{SS}$ is also shown in Table 2 and Fig. 5. Increase in effective barrier height Φ_e of both the diodes in forward bias is observed. This may be due to the increase in quasi-Fermi energy level of the majority carriers on the semiconductor side. This causes most of the electrons to be injected directly into the metal forming a thermionic emission current, while some of them are trapped by the interface states. This charge capture process results in an increase in effective barrier height thereby reducing the diode current [19,27,29].

The interface state density as determined by Terman's method is found to be 3.79×10^{12} and 3.41×10^{10} cm^{-2} eV^{-1} for the MS and MIS Schottky diodes, respectively [34]. From Fig. 5, it can be seen that an exponential increase in interface states density exists from mid gap towards the bottom of the conduction band. This rise is less significant for the MIS diode compared to that of the MS diode. At any specific energy, the interface states density of the MIS diode is lower when compared to that of the MS diode,

Table 2
Interface states energy distributions obtained from the forward bias I–V characteristics at 300 K for MS and MIS diodes.

Voltage (V)	n	Φ_e (eV)	$E_C - E_{SS}$ (eV)	$N_{SS} \times 10^{16}$ (eV^{-1} m^{-2})
MS				
0.08633	1.11745	0.79907	0.71274	2.43176
0.1367	1.08406	0.8006	0.6639	1.73073
0.187	1.10238	0.80737	0.62037	2.11537
0.2374	1.1296	0.81724	0.57984	2.68684
0.2878	1.15525	0.82868	0.54088	3.22522
0.3381	1.18025	0.84163	0.50353	3.75004
0.3885	1.2027	0.85548	0.46698	4.22132
0.4388	1.22392	0.87028	0.43148	4.66674
0.4892	1.24361	0.88583	0.39663	5.08021
0.5396	1.26165	0.90191	0.36231	5.4588
0.59	1.27851	0.91852	0.32852	5.8127
0.6403	1.29478	0.93578	0.29548	6.15433
0.6906	1.31113	0.95388	0.26328	6.4975
0.741	1.32878	0.97334	0.23234	6.86805
0.7914	1.34678	0.99378	0.20238	7.24597
0.8418	1.36775	1.01634	0.17454	7.68625
0.8921	1.39105	1.04078	0.14868	8.17523
0.9424	1.41714	1.0674	0.125	8.72304
0.9928	1.44725	1.09681	0.10401	9.35516
1.043	1.48	1.12827	0.08527	1.00426
MIS				
0.08633	1.29547	0.87969	0.79336	0.30256
0.1367	1.16343	0.8792	0.7425	0.16396
0.187	1.1602	0.88582	0.69882	0.16058
0.2374	1.19057	0.898	0.6606	0.19246
0.2878	1.24569	0.91676	0.62896	0.25031
0.3381	1.29395	0.93681	0.59871	0.30097
0.3885	.33775	0.95809	0.56959	0.34694
0.4388	1.37855	0.98049	0.54169	0.38976
0.4892	1.415	1.00348	0.51428	0.42803
0.5396	1.45017	1.02751	0.48791	0.46494
0.59	1.48169	1.05181	0.46181	0.49802
0.6403	1.51003	1.07627	0.43597	0.52776
0.6906	1.53679	1.10122	0.41062	0.55586
0.741	1.56043	1.12613	0.38513	0.58067
0.7914	1.58295	1.15145	0.36005	0.60431
0.8418	1.60359	1.17685	0.33505	0.62597
0.8921	1.62169	1.202	0.3099	0.64497
0.9424	1.64023	1.22785	0.28545	0.66443
0.9928	1.65713	1.25369	0.26089	0.68217
1.043	1.67389	1.2799	0.2369	0.69976

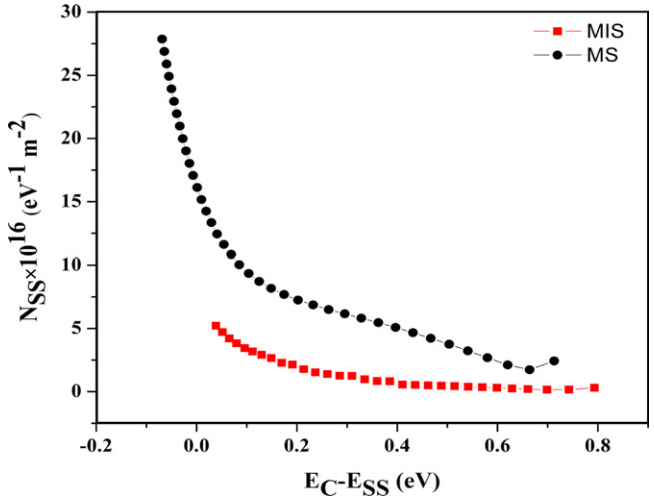

Fig. 5. Interface state density distribution profiles as a function of $E_C - E_{SS}$ for MS and MIS diodes.

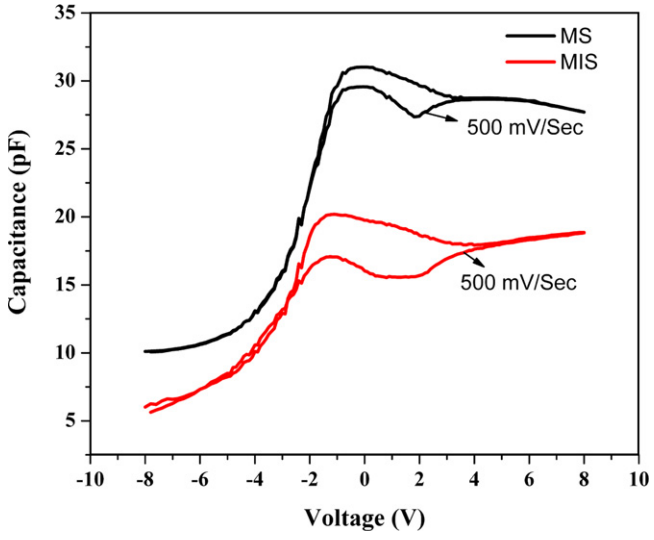

Fig. 6. MOS C–V measurements of Au/n-GaN MS and Au/SiO_2/n-GaN MIS diodes at 1 MHz.

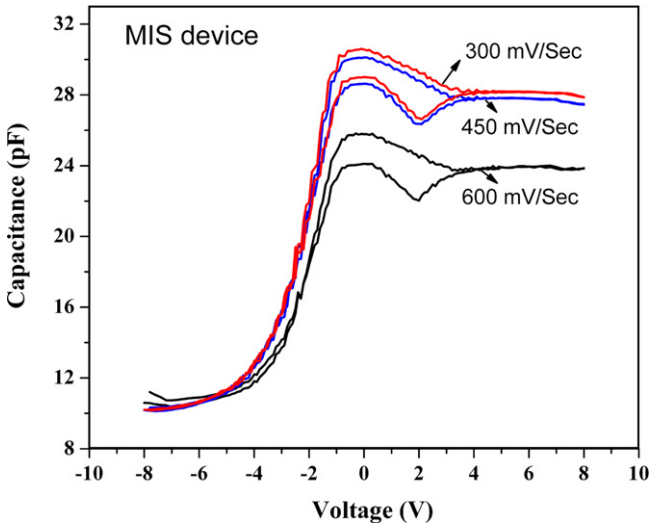

Fig. 7. The MOS *C–V* measurement with bias sweep rates of 300, 450, 600 mV/s for MIS Schottky diodes.

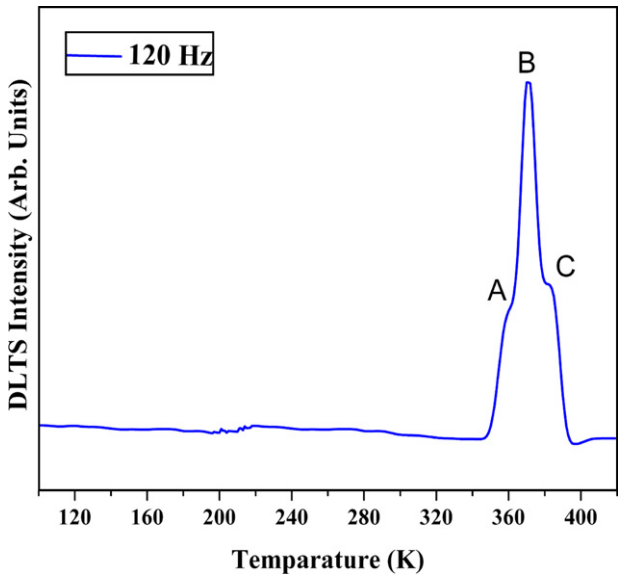

Fig. 8. DLTS spectra for electron traps in the Au/SiO_2/n-GaN MIS diode ($V_r = -1$ V, $V_p = 0.5$ V, $t_p = 100$ μs, $f = 120$ Hz).

which may be due to the fact that MIS diode has a thick oxide layer than that of the MS diode [19,27,35,36] because of the saturation of dangling bonds.

Fig. 6 shows MOS *C–V* characteristics of MS and MIS diodes measured from DLS-83D spectrometer at 1 MHz. A small injection type hysteresis loop is seen in MS and MIS Schottky diodes. The increase in loop width after insulating layer confirms the reduction in the interface state density at the oxide-semiconductor junction. The MOS *C–V* measurements of the MIS diode at different sweep rates of 300, 450 and 600 mV/s from 8 V to −8 V and then back to +8 V is shown in Fig. 7. The interface state density calculated from Terman's method is found to be increased with sweep rate. The interface densities are 2.47×10^{11} cm^{-2} eV^{-1}, 3.35×10^{11} cm^{-2} eV^{-1} and 3.5×10^{11} cm^{-2} eV^{-1} for the sweep rates of 300, 450 and 600 mV/s, respectively. In the slower bias sweep rate, more electrons were trapped in the deep interface states and larger amount of interface traps can be charged. The emission time constant of the relatively deeper states is so long that almost no trapped electrons can be emitted. The hysteresis observed in MIS diodes for different sweep rates is mainly caused by the charging and discharging of electrons from the relatively shallow interface traps [37].

In the *C–V* measurements, there is a discrepancy observed in the doping concentration determined from MS and MIS diodes. This reduction could be due to the traps associated with the oxide layer. DLTS measurements are used to find out the trap carrier concentration and the activation energy of the trap. In order to characterize the deep level defects, DLTS measurements are performed over the temperature range 100–400 K using automated DLTS system. Typically, a quiescent reverse bias of $V_r = -1$ V is employed with filling-pulse voltage $V_p = +0.5$ V and filling pulse width $t_p = 100$ μs. The thermal activation energy E_T of electron trap is determined from the thermal emission rate e_n for electron from the deep level into the conduction band [38]

$$e_n = \sigma_n \nu_{th} N_c \exp\left(\frac{-E_T}{k_T}\right) = \frac{1}{\tau_e} \quad (14)$$

here σ_n is the capture cross-section, ν_{th} is the thermal velocity of an electron defined as $\nu_{th} = (3kT/m_{eff})^{1/2}$, N_c is the effective density states at the bottom of the conduction band, k is the Boltzmann's constant, T is the absolute temperature and τ_e is the emission rate constant, which is the reciprocal of the emission rate e_n. Fig. 8 shows the DLTS spectra of the MIS diode. Three DLTS peaks are identified which are labeled as *A*, *B* and *C*. The trap *B* is a narrow peak in DLTS spectra. This peak shape could be attributed to non-exponential transients due to the formation of dislocations or dislocation-related defects in semiconductor materials as a result of the repulsive Coulombic barriers associated with such defects. Slow and non-exponential transients in the case of n-GaN MIS Schottky diode have been ascribed to surface states. In our case the presence of interface states is confirmed by the observation that when the bias is swept forth and back from accumulation to deep depletion, a counterclockwise hysteresis is observed in the *C–V* curves measured on the MIS Schottky diodes. The presence of interface states that capture electrons during the accumulation bias and then emit carriers when this bias is removed. The thermal activation energy for electron emission from each deep level is determined from an Arrhenius analysis of the emission time constant. From several such spectra, the product $e^{-1}{}_n \nu_{th} N_c$ can be calculated and plotted as function of 1000/*T*, leading to the straight line in an Arrhenius plot. Fig. 9 shows an Arrhenius plot for *A*, *B* and *C*

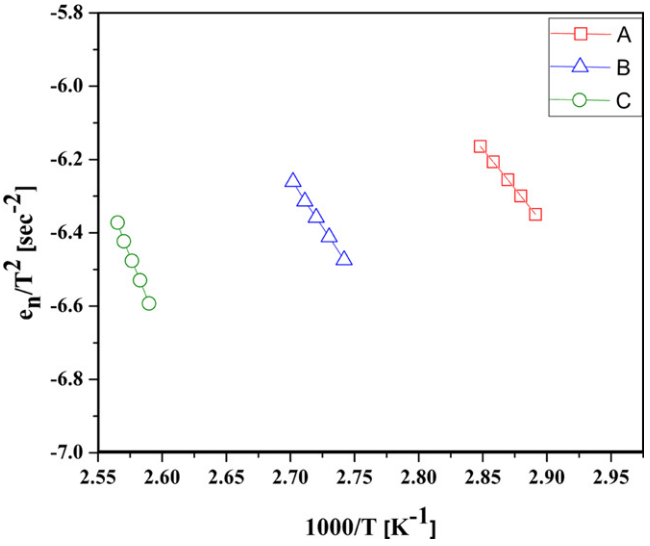

Fig. 9. Arrhenius plots of emission rate and temperature for the three deep level defects for Au/SiO_2/n-GaN MIS diode.

deep levels from which we obtain the following activation energies $A = 0.38 \pm 0.01$, $B = 0.46 \pm 0.01$ and $C = 0.76 \pm 0.01$ below the conduction band. We suggest that our level C corresponds to the defect level with activation energy of 0.77 eV reported by Nakano and Jimbo [9] in sputtered SiO_2/GaN MOS samples. This interface trap probably induces the Fermi level pinning effect at the SiO_2/GaN interface [9,39,40].

The uniform defect concentration N_T is determined using DLTS signal at emission peaks is shown in Fig. 8. The defect concentration can be calculated using the expression given by

$$N_T = 2N_D \cdot \frac{\Delta C}{C} \quad (15)$$

where N_T is the trap concentration, ΔC the capacitance change due to saturation injection pulse, C the capacitance of the diode under quiescent reverse bias condition and N_D the donor concentration. The calculated trap carrier concentration for trap A is $7.68 \times 10^{15}\,cm^{-3}$ for trap B $2.16 \times 10^{14}\,cm^{-3}$ and for trap C $3.89 \times 10^{15}\,cm^{-3}$. These trap densities are indeed small in comparison with the shallow donor densities.

4. Conclusions

In conclusion, the interface properties of Au/n-GaN and Au/SiO_2/n-GaN Schottky diodes have been investigated by current–voltage, capacitance–voltage and DLTS measurement techniques. The calculated value of the barrier height for MS and MIS Schottky diodes are found to be 0.79 eV (I–V), 0.87 eV (C–V) and 0.86 eV (I–V), 0.99 eV (C–V), respectively. It is observed that the saturation current (I_o) is reduced in the MIS diode as compared to the MS diode. The reduction in the saturation current in the MIS case is caused by the thin oxide layer and is due to a combination of increased barrier height and reduced velocity of charge carriers. The barrier height increase is ascribed to a negative charge at the interface, while recombination in the oxide is presumed to be the cause of the latter. The calculated interface densities are $2.47 \times 10^{11}\,cm^{-2}\,eV^{-1}$, $3.35 \times 10^{11}\,cm^{-2}\,eV^{-1}$ and $3.5 \times 10^{11}\,cm^{-2}\,eV^{-1}$ for the sweep rates of 300, 450 and 600 mV/s from MOS C–V measurements for the MIS Schottky diode. The interface state density calculated from Terman's method is found to be increased with sweep rate. From the reverse bias C–V measurement, it is observed that the doping concentration decreases in MIS diodes as compared with that of MS diode. This may be due to the presence of thin oxide layer. Based on the DLTS results, the dominant interface trap is found to be located at ~0.76 eV below the conduction band. Therefore, this interface trap is considered to induce the surface Fermi-level pinning at the SiO_2/GaN interface.

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